A ZERO-BIAS GaAs MILLIMETER WAVE INTEGRATED DETECTOR CIRCUIT

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ABSTRACT

A monolithic GaAs millimeter wave diode detector circuit has been developed. A novel zero-bias detector diode is integrated with Ta_2N resistors and a Si_3N_4 capacitor on a chip 440 μm x 500 μm in size. Excellent detector performance has been demonstrated through 40 GHz.

Introduction

Millimeter wave detectors have employed point-contact silicon diodes (whisker type) almost exclusively for a long time. This is because the bonding wire parasitics in alternative diode structures limit performance at higher frequencies. The point-contact detectors, however, are difficult to assemble and they lack ruggedness. The whisker diode performance is a strong function of the diode area, whisker configuration and pressure on the diode. The performance of each diode must be individually obtained by adjusting the whisker position and pressure. Performance can change accordingly when the diode is subject to shock or vibration. Development of more reliable detector structures with competitive electrical performance at mm wave frequencies was thus warranted.

In this paper we will describe our development work of a millimeter wave GaAs monolithic detector circuit (Fig. 1), on which a planar, zero-bias Schottky barrier GaAs diode is integrated with two Ta_2N thin film resistors (for 50-ohm input termination) and a Si_3N_4 thin film by-pass capacitor (10 pF). The total chip size is 440 μm x 500 μm.

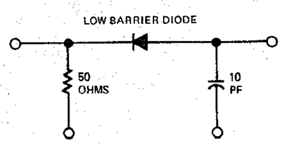

Fig. 1. mm Wave Detector Circuit Schematic

To the best of our knowledge, a technology providing low barrier GaAs Schottky detector diodes with on-chip integration for mm wave detection is pioneering work.

The chip integration provides reduced interconnect parasitics and improved input match as well as more uniform and more reproducible circuit performance. Another more important contribution is the novel method used in lowering the Schottky barrier height of GaAs to such a low value that state of the art zero-bias detection is achieved. The lowering scheme will be briefly presented in this report.

Fabrication

Figure 2a shows the structural details of the circuit components. The starting material is N/N^+ LPE double layers, which are grown on a semi-insulating GaAs substrate. The N^+ layer ($N_D > 10^{18}$ cm^{-3}) is used to minimize the diode spreading resistance. The conductive diode area is isolated from the other circuit elements by proton bombardment of the GaAs field using a gold mask. A sputtered Ta_2N thin film of 50 ohms/

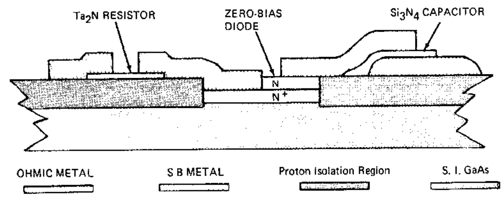

Fig. 2a. Detector Circuit Structural Detail.

square is used for the matching resistors and Ge/Au is used for the diode ohmic contact. Plasma deposited Si_3N_4 is then put down between the ohmic and Schottky metal layers to form the by-pass capacitor. In addition, the Schottky (anode) metal is also used to connect the on-chip resistors, capacitor and diode. Fig. 2b shows the processed detector chip.

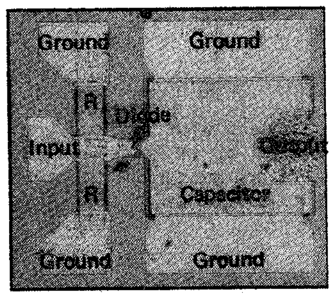

Fig. 2b. Micrograph of the Detector Chip.

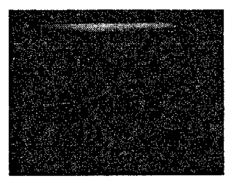

Fig. 3. I–V Characteristics of a GaAs Zero–Bias Diode.

The normal Schottky barrier height of n-type GaAs is about 0.8 eV. To use the GaAs diode in mm wave detection, a bias of at least 0.8 Volt is needed to maintain near optimum detector sensitivity. In many detector applications, however, a zero-bias diode circuit is highly desirable and sometimes absolutely necessary. In our work we achieved the diode barrier lowering by using a unique Schottky barrier metal system (Sn-Ge-Au), in which the barrier height can be lowered to a desired level by sintering after metal deposition. The barrier lowering mechanism is believed to be due to the formation of a very thin, but heavily doped N^+ layer near the metal/GaAs interface.[1,2] The detector characteristics of our GaAs diode processed in the manner described here are similar to the best commercial available zero-bias silicon diodes, and the diode circuit maintains these characteristics to frequencies greater than 40 GHz. Figure 3 shows the I-V diode characteristics of our low barrier zero-bias diode near the origin.

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Performance

The monolithic detector circuit with a 10 μm^2 active diode area has the following measured parameters:

(1) The diode junction capacitance $C_j \approx 0.05$ pF

(2) The diode video resistance ($\frac{dV}{dI}$ at origin) $R_v \approx 1$ KΩ

(3) The diode spreading resistance $R_s \leq 30\ \Omega$

(4) A quantity used to calculate the detector sensitivity $S = \left(\frac{d^2I}{dV^2}\right) / \left(\frac{dI}{dV}\right) \Big|_{V \sim 0} \geq 10\ V^{-1}$.

The mm wave performance from 26.5 to 40 GHz is summarized in the following:

(1) Voltage sensitivity $\Gamma \geq 0.3$ mV/μW

(2) Tangential sensitivity $T_{ss} \leq -47$ dBm (measured with 100 KHz BW and 3 dB amplifier noise figure).

(3) Return loss $\geq$ 12 dB

(4) Flatness $\pm$ 1 dB

Figure 4 shows the return loss and the flatness as a function of frequency. It is notable that there is no sign of performance degradation beyond 40 GHz. We thus believe that the circuit will be useable far beyond 40 GHz.

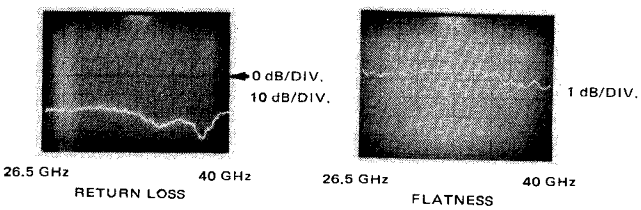

Fig. 4. Return Loss and Flatness Measurements.

Circuit Testing

The detector tangential sensitivity (T_{ss}) and voltage sensitivity (Γ) are usually directly measured in a waveguide circuit. The test, however, is both time consuming and costly because the die must be attached and bonded in the waveguide circuit. To alleviate these problems and to provide chip by chip testing on the wafer, a computer aided test system was devised. The block diagram of the system is shown in Fig. 5. The system measures the DC parameters on the chip and then calculates the RF performance (Γ, T_{ss}, etc.) using the model shown in the appendix. Each die on the wafer may thus be individually screened for a particular desired microwave performance.

Figure 6 demonstrates the success of this procedure by showing the very good agreement achieved between calculated Γ and T_{ss} and the actual measured microwave values on a number of chips.

Microwave Measurement

To measure the microwave performance, the diode chip is mounted into a cartridge with a coaxial input (Fig. 7). A stepped waveguide to coaxial transition with > 30 dB return loss, couples the Ka-band waveguide to the 2.9 mm coaxial line. The input of the

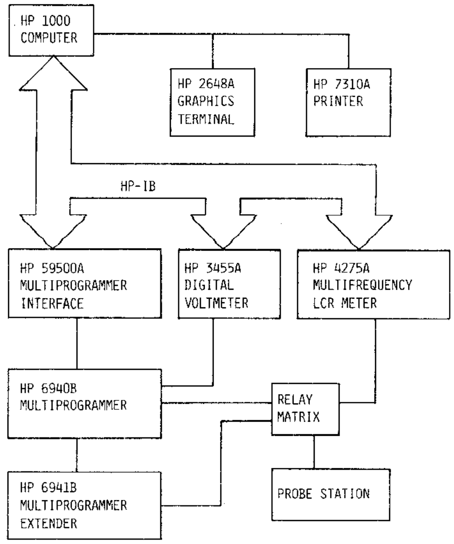

Fig. 5. Computer Aided Measurement System.

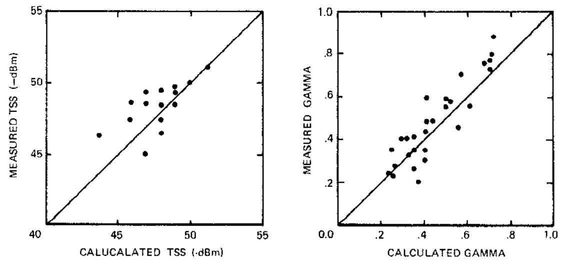

Fig. 6. Agreement of Measured T_{ss} and Γ vs Calculated Values.

cartridge has a glass to metal seal for hermeticity. That seal exhibits $\gtrsim$ 20 dB return loss, and is a significant contribution to the overall return loss of the device.

We measure the return loss with the Ka-band waveguide reflectometer set-up shown in Fig. 8a. When measuring a 20 dB return loss, the uncertainty is typically ±1 dB.

The detector flatness is measured using the waveguide power splitter leveled source shown in Fig. 8b. The Thermistor mount and the waveguide splitter were characterized together as a unit and the overall system measures flatness with better than ±0.25 dB uncertainty.

Typical measured data, using the described setups, are shown in Fig. 4.

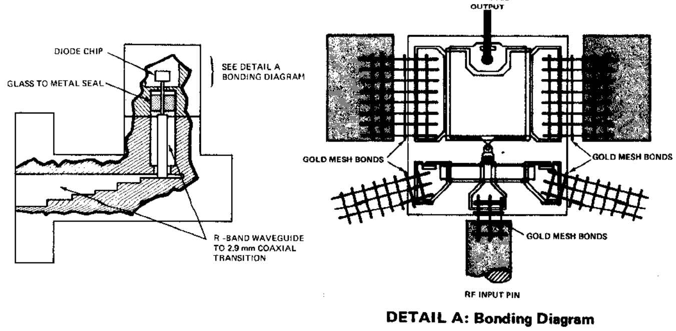

Fig. 7. RF Preformance Measurement.

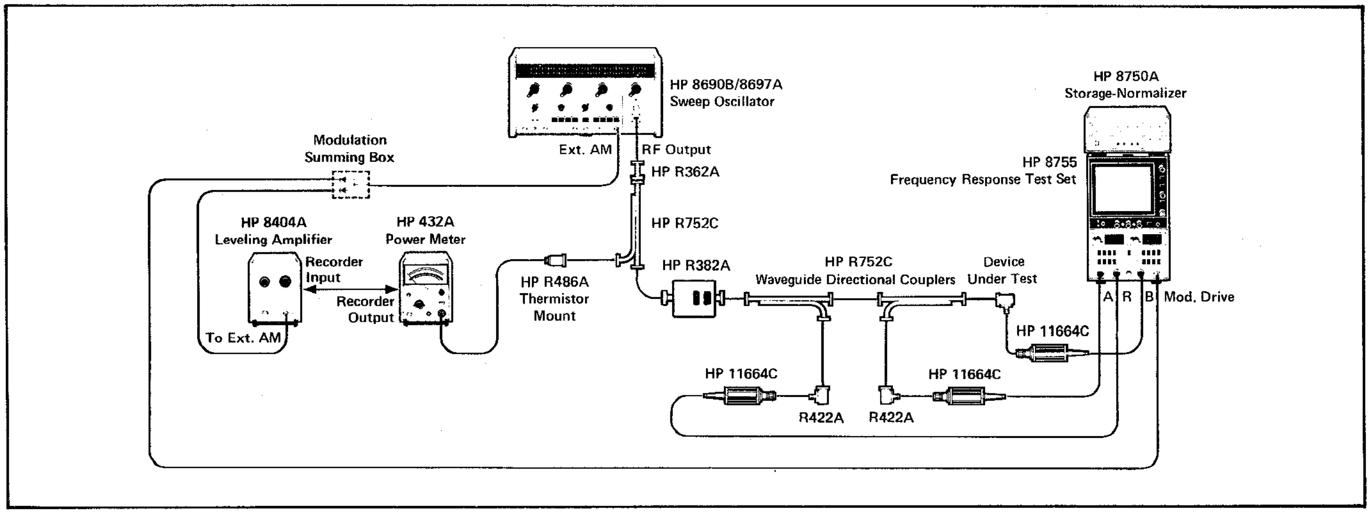

Fig. 8a. Test Setup for Return Loss Measurement.

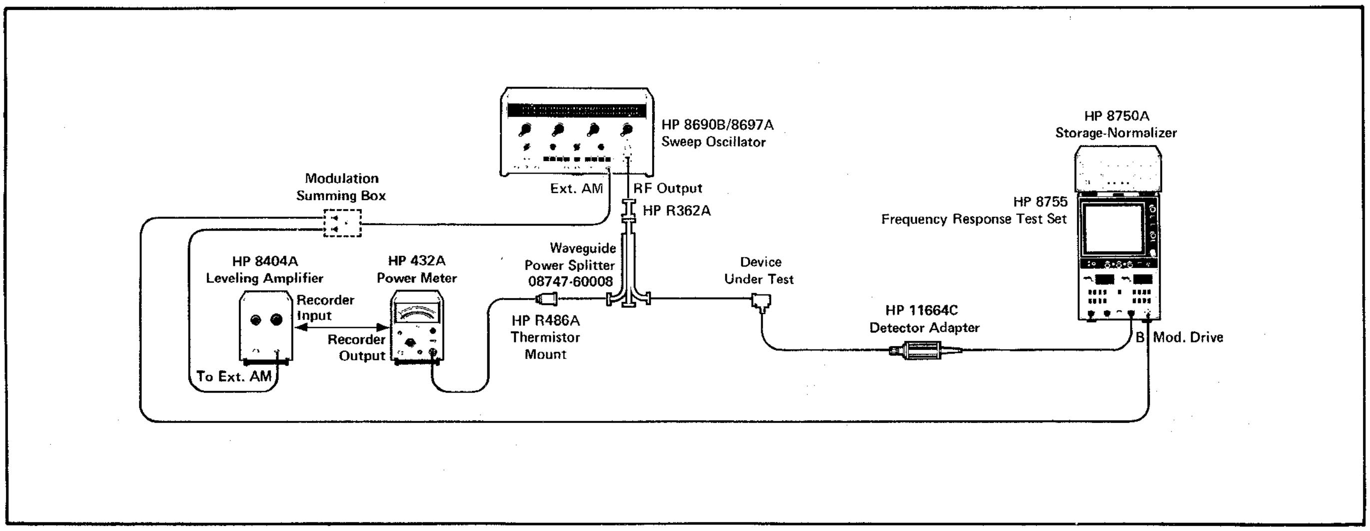

Fig. 8b. Test Setup for Flatness Measurement.

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Appendix

The usual relationship of the voltage (Γ) and current (β) sensitivities $\Gamma = \beta R_v$ should be corrected to $\Gamma = \beta R_v\,(Z_0/R_r)$ due to the power splitting at microwave frequency. The factor (Z_0/R_r) is the ratio of the power delivered to the diode to that available at the input port where R_r is the real part of the diode equivalent circuit, and Z_0 the characteristic impedance. By measuring the usual diode parameters (R_v, R_s, and C_j), R_r can be calculated easily. The microwave β can also be calculated from β_0 and the measured diode parameters. The value β_0 is determined as the optimal point of

$$\left(\frac{d^2I}{dV^2}\right)/\left(\frac{dI}{dV}\right)$$ by measuring it near zero bias condition. Then

$$\beta = \beta_0 \left(\frac{1}{1 + \frac{\omega^2 C_j^{\,2}\, R_v^{\,2} R_s}{R_v + R_s}}\right)$$

Thus the tangential sensitivity T_{ss} is calculated as usual

$$T_{ss} = 10 \log_2 NDS + 4 \qquad \text{(dBm)}$$

where $NDS = \frac{2}{\Gamma}\sqrt{KTBF}$ (Nominal Detectable Signal)

In our case B = 100 KHz and F = 2.